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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,999	02/14/2002	Ken Takeuchi	001701.00140	9741

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EXAMINER	
HO, HOAI V	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 11/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EL

Office Action Summary	Application No.	Applicant(s)	
	10/073,999	TAKEUCHI ET AL.	
	Examiner	Art Unit	
	Hoai V. Ho	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *47-60,62,63,65 and 66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *47-60,62,63 and 65-66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/667,610.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This office acknowledges receipt of the following items from the Applicant:

RCE

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/11/05 has been entered.

2. Claims 47-60, 62, 63, and 65-66 are presented for examination.

Claim Rejections - 35 USC 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 47-60, 62, 63, and 65-66 are rejected under 35 U.S.C. 102(a) as being anticipated by Hemink et al. U.S. Pat. No. 5,870,334 (IDS).

Regarding to claims 47-50, 55-57 and 59, 60, 62, 63, 65 and 66, Figures 8, 13 and 20 (col. 16, lines 17-20 and 28-31) of Hemink is directed to a nonvolatile semiconductor memory comprising: a first memory cell section (M1-M4 of upper and lower of a first string connect to a first main bit line BL in fig. 8, M1 in fig. 13 or M11 in fig. 20) including a first memory cell; a first bit line (a upper section of M1-M4 connects to a switch transistor S2 in fig. 8) connected to said first memory cell section; a second bit line (a lower section of M1-M4 connects to a switch transistor S2 in fig. 8); a second memory cell section (M1-M4 of upper and lower of a second

string connect to second main bit line BL in fig. 8) including a second memory cell (M1 or M4 in fig. 8, or another memory cell connects in parallel with M1, M12); a third bit line (a upper section of M1-M4 in the second string connects to a switch transistor S2 in fig. 8, a common connection of transistors of another latch as Qn3 and Qn5 in fig. 13) connected to said second memory cell section; fourth bit line (a lower section of M1-M4 in the second string connects to the switch transistor S2 in fig. 8, or a common connection of transistors as Qn6 and Qn7 of another capacitor); and a common latch circuit (103, FF. col. 10, lines 26-38) connected to one ends (through the switch transistor S2) of said first, second, third and fourth bit lines, latching program / read data of at least one said first and third memory cells, wherein said first, second, third and fourth bit lines are different (by switch transistor S2) from each other; said first and second memory cells are programmed substantially simultaneously (controls by the same word line signal CG1, col. 14, lines 30, 31, 42 and 43), program data of said first memory cell is held by at least one of said first and second bit lines, and program data of said second memory cell is held by at least one of said third and fourth bit lines while a program voltage is supplied to said first and second memory (M2 or M21) cells (col. 10, line 24 to col. 11, line 20); a verify read operation to verify whether said first memory cell has been sufficiently programmed, is carried out by said common latch circuit, and program data of said third memory cell is held by said fourth bit line while conducting the verify read operation of said first memory cell; and said common latch circuit and said fourth bit line are electrically connected to each other, after the program data of said second memory cell held by said fourth bit line is transferred to said common latch circuit, a verify read operation to verify whether said second memory cell has been sufficiently programmed, is carried out using the program data of said second memory cell

held by said common latch circuit, and while conducting a verify read operation of said second memory cell, the program data of said first memory cell is held by said second bit line (col. 11, lines 21-24).

Regarding to claims 51-54, Figure 13 or 20 of Hemink discloses wherein said first memory cell (M1or M21) and said second memory cell (M2 of fig. 13 or M21 of fig. 20) are connected to different word lines (CG1 and CG2).

Regarding to claim 58, Figure 13 or 20 of Hemink discloses wherein said first (M1 of fig. 13 or M11 of fig. 20) and second memory (another memory cell connects in parallel with M1 or M12) cells are connected to a same word line (CG1).

5. Claims 47-60, 62, 63, and 65-66 are rejected under 35 U.S.C. 102(e) as being anticipated by Sakui et al. U. S. Patent No. 6307807 (PTO 892 see Mail Date 0404).

Figure 38 of Sakui is directed to a nonvolatile semiconductor memory comprising: a first memory cell section (MEMORY CELL UNIT BLi) including a first memory cell; a second memory cell section (MEMORY CELL UNIT /BLi) including a second memory cell; a first bit line (BLi) connected to said first memory cell; a second bit line (/BLi) connected to said second memory cell, being different from the first signal line; and a common latch circuit (SENSE AMPLIFIER) connected to one ends of said first and second bit lines; wherein first program/read data of said first memory cell (controlling by a signal φa) is latched in said common latch circuit, while second program/read data of said second memory cell is held by said second bit line (controlling by a signal φb).

6. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

7. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1777.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is (571)-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

H. Ho
November 3, 2005

Hoai V. Ho
Primary Examiner
Art Unit 2827.